IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Applicant: Jason M. Howard et al.

Title: MULTI-THREADED MULTIPLY ACCUMULATOR

Docket No.: 884.584US1
Filed: February 8, 2002
Examiner: Chat C. Do

Serial No.: 10/071,373
Due Date: May 24, 2006
Group Art Unit: 2193

MS Appeal Brief - Patents
Commissioner for Patents
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Amy Moriarty
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(GENERAL)

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Jason M. Howard et al. Examiner: Chat C. Do

Serial No.: 10/071,373 Group Art Unit: 2193

Filed: February 08, 2002 Docket: 884.584US1

For: MULTI-THREADED MULTIPLY ACCUMULATOR

Assignee: Intel Corporation

APPEAL BRIEF UNDER 37 CFR § 41.37

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Commissioner for Patents
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Alexandria, VA 22313-1450

Sir:

The Appeal Brief is presented in support of the Notice of Appeal to the Board of Patent Appeals and Interferences, filed on January 20, 2006, from the Final Rejection of claims 8-30 of the above-identified application, as set forth in the Final Office Action mailed on September 20, 2005.

The Commissioner of Patents and Trademarks is hereby authorized to charge Deposit Account No. 19-0743 in the amount of 500.00 which represents the requisite fee set forth in 37 C.F.R. § 41.2(b)(2). The Appellants respectfully request reconsideration and reversal of the Examiner's rejections of the pending claims.

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APPEAL BRIEF UNDER 37 C.F.R. § 41.37

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1. REAL PARTY IN INTEREST

The real party in interest of the above-captioned patent application is the assignee, INTEL CORPORATION.

2. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellants that will have a bearing on the Board's decision in the present Appeal.

3. STATUS OF THE CLAIMS

The present application was filed on February 8, 2002 with claims 1-30. A non-final Office Action was mailed February 10, 2005, which included a restriction requirement to which the Appellants' representatives had made an earlier provisional election via a telephone interview. A Final Office Action was mailed September 20, 2005. Claims 8-30 stand rejected, remain pending, and are the subject of the present Appeal.

4. STATUS OF AMENDMENTS

No amendments have been made subsequent to the Final Office Action dated September 20, 2005.

5. SUMMARY OF CLAIMED SUBJECT MATTER

Some aspects of the present inventive subject matter include, but are not limited to an integrated circuit such as integrated circuit 200 as illustrated in FIG. 2 comprising a multiplier such as 232 coupled to receive interleaved operands and to produce a product; and a multi-threaded accumulator such as multi-threaded accumulator circuit 100 coupled to the multiplier to receive the product. *Page 5, line 18 through page 6, line 12.*

Some aspects of the present inventive subject matter include, but are not limited to an accumulator circuit such as circuit 100 as illustrated in FIG. 2, to accept operands from different threads interleaved in time, the accumulator having intermediate registers to simultaneously hold partial results from each of the different threads. *Page 3, line 2 through page 6, line 12.*

Some aspects of the present inventive subject matter include, but are not limited to a multi-threaded floating point multiply-accumulator circuit such as multi-threaded floating point multiply accumulate circuit 300 as illustrated in FIG. 3, comprising a multiplier to produce a product; and an accumulator coupled to receive the product from the multiplier, the accumulator including sequential elements to provide a multi-threaded capability. *Page 3, line 20-29; page 6, line 27 through page 7, line 4; page 15, lines 6-9.*

This summary does not provide an exhaustive or exclusive view of the present subject matter, and Appellants refer to the appended claims and its legal equivalents for a complete statement of the invention.

6. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 8-9, 15-16, and 19-23 were rejected under 35 U.S.C. § 102(b) as being anticipated by Chip et al. ("The Coreware Methodology: building a 200 Mflop processor in 9 man month's").

Claims 10-11 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Chip et al. ("The Coreware Methodology: building a 200 Mflop processor in 9 man month's") in view of Debabrata et al. ("A 600 MHz half-bit level pipelined accumulator-interleaved multiplier accumulator core").

Claims 12-14, 17-18, and 24-30 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Chip et al. ("The Coreware Methodology: building a 200 Mflop processor in 9 man month's") in view Choquette (U.S. 6,480,872).

7. ARGUMENT

A) The Applicable Law under 35 U.S.C. §102(b)

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. M.P.E.P § 2131. To anticipate a claim, a reference must disclose every element of the challenged claim and enable one skilled in the art to make the anticipating subject matter. *PPG Industries, Inc. V. Guardian Industries Corp.*, 75 F.3d 1558, 37 USPQ2d 1618 (Fed. Cir. 1996). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

B) Discussion of the rejection of claims 8-9, 15-16, and 19-23 under 35 U.S.C. § 102(b) as being anticipated by Chip et al.

Claims 8-9, 15-16, and 19-23 were rejected under 35 U.S.C. § 102(b) as being anticipated by Chip et al. (Chip Stearns, et al., *The Coreware Methodology: Building a 200 Mflop Processor in 9 Man Months,* IEEE, 549 (Sept. 1992)). Appellants respectfully traverse the rejection of claims 8-9, 15-16, and 19-23 because Chip et al. fails to teach each of the elements included in claims 8-9, 15-16, and 19-23, and so the Final Office Action fails to state a *prima facie* case of anticipation with respect to claims 8-9, 15-16, and 19-23.

Chip et al. discloses operations on ordinate transformations in parallel for computer graphics. However, a disclosure of transformations in parallel fails to teach interleaved operands, and fails to teach multi-threaded operations, as included in Appellants' claimed invention. Chip et al.'s disclosure of "effectively interleaving" a multiplier and an adder as further described below is not the same as receiving actually interleaved operands at the multiplier, as recited in the claims of the present application.

For example, claim 8 recites, "a multiplier coupled to receive interleaved operands and to produce a product; and a multi-threaded accumulator coupled to the multiplier to receive the product." (Emphasis added). In the specification of the present application on page 5, lines 25-29 it states,

> As a result, the operands on nodes 217 and 218 are interleaved between the sets $\{A_i, B_i\}$ and $\{C_j, D_j\}$. Multiplier 232 receives the interleaved operands on nodes 217 and 218, multiplies them, and produces a data stream on node 102 interleaved between the products (A_iB_i) and (C_jD_j).

Thus, claim 8 recites a multiplier coupled to receive interleaved operands. In contrast, Chip et al. on page 550, right hand column at lines 5-12 recites,

> In this case, shown in Figure 2, a 4-stage pipe exists in both the multiplier and the adder. The pipe stages allow the arithmetic cores to operate on four ordinate transformations in parallel. The floating-point multiplier and adder are effectively interleaved, with each stage transforming one coordinate in the vertex. Table 2 shows how the interleaved scheme transposes the order of the operations to match the latency of the architecture. (Emphasis added).

Having a multiplier and adder "effectively interleaved," and transposing the order of the operations to match the latency of the architecture, as disclosed in Chip et al., fails to teach receiving interleaved operands, as recited in for example in claim 8 as quoted above. Receiving interleaved operands involves alternating the input streams in time to the same device such as a multiplier. (*See* e.g. Appellants' specification on page 3 at lines 9-12). A disclosure of "effectively interleaving" a multiplier and an accumulator fails to disclose receiving interleaved operands because "effectively interleaving" two devices is not the same as receiving interleaved operands. Chip et al. merely shows operations on a series of operands, first including χ and then y, and transposing the order of the operations to match the latency of the architecture, but fails to teach "a multiplier coupled to receive interleaved operands" as recited in claim 8.

Claim 8 also includes a multi-threaded accumulator. In contrast, Table 2 of Chip et al. discloses an entry where "ax + by" is performed in the "Adder Operation".

Therefore, any operations including χ and y are combined in the adder of Chip et al., and therefore cannot be multi-threads, as recited in claim 8. Multiple threads are sets of operands that produce different products and are maintained as separate entities throughout the operations performed on these sets of operands as they pass through the multi-threaded accumulator. In Chip et al., operands χ and y are shown as combined in the "Adder Operation," and thus are not multi-threaded as recited in claim 8.

Therefore, Chip et al. fails the teach each of the elements of claim 8, and so the Final Office Action fails to state a *prima facie* case of anticipation with respect to claim 8, and also with respect to dependent claims 9 and 15 that depend from claim 8.

In another example, claim 16 recites, "the accumulator having intermediate registers to simultaneously hold partial results from each of the different threads." (Emphasis added). In a further example, claim 23 recites, "the accumulator including sequential elements to provide a multi-threaded capability." (Emphasis added).

As noted above, Chip et al. on page 550, in the right hand column at lines 5-7 recites, "in Figure 2, a 4-stage pipe exists in both the multiplier and the adder." However, Chip et al. fails to teach the elements of claims 16 and 23 as quoted above because Chip et al. goes on to state on page 550, in the right hand column at lines 7-8, "The pipe stages allow the arithmetic cores to operate on four ordinate transformations in parallel." (Emphasis added).

Therefore, with regards to claims 16, the four separate registers relied on in the Final Office Action on page 3 represent registers operating in parallel on four ordinate transformations. Operating in parallel does not teach operations on multiple threads, and thus does not teach "the accumulator having intermediate registers to simultaneously hold partial results from each of the different threads," as recited in claim 16. (Emphasis added).

Operations in parallel also fails to teach a multi-threaded capability, as recited in claim 23. The specification of the present application on page 5 at lines 1-2 states, "Accumulator circuit 100 is a 'multi-threaded' accumulator because it operates on two 'threads' simultaneously." Further, as noted above, the specification of the present

invention on page 5, lines 25-26 states, "As a result, the operands on nodes 217 and 218 are interleaved between the sets $\{A_i, B_i\}$ and $\{C_j, D_j\}$."

As argued above with regards to claim 8, Chip et al. does not receive interleaved operands at the multiplier. Since Chip et al. does not receive interleaved operands (multi-threaded) at the multiplier, Chip et al. does not teach the accumulator having intermediate registers to simultaneously hold partial results from each of the different threads, as recited in claim 16, and does not teach multi-threaded capability, as recited in claim 23.

In contrast and as noted above, Chip et al. discloses, "arithmetic cores to operate on four ordinate transformations in parallel." Again, a disclosure of "parallel" operations fails to teach the multi-thread operations of the presently claimed subject matter.

Therefore, Chip et al. fails the teach each of the elements of claims 16 and 23, and so the Final Office Action fails to state a *prima facie* case of anticipation with respect to claims 16 and 23, and also with respect to dependent claims 19-22 that depend from claim 16.

For at least the reasons stated above, Appellants respectfully request reversal of the rejection, and reconsideration and allowance of claims 8-9, 15-16, and 19-23.

C) The Applicable Law under 35 U.S.C. §103(a)

The Examiner has the burden under 35 U.S.C. § 103 to establish a *prima facie* case of obviousness. *In re Fine*, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). As part of establishing a *prima facie* case of obviousness, the Examiner must show that some objective teaching in the prior art or some knowledge generally available to one of ordinary skill in the art would lead an individual to combine the relevant teaching of the references. *Id.*

The court in *Fine* stated that:

> Obviousness is tested by "what the combined teaching of the references would have suggested to those of ordinary skill in the art." *In re Keller*, 642 F.2d 413, 425, 208 USPQ 871, 878 (CCPA 1981)). But it "cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination." *ACS Hosp. Sys.*, 732 F.2d at 1577, 221

USPQ at 933. And "teachings of references can be combined *only* if there is some suggestion or incentive to do so." *Id.* (emphasis in original).

The M.P.E.P. adopts this line of reasoning, stating that,

> "To establish a *prima facie* case of obviousness, three base criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991))". *M.P.E.P.* § 2142.

The test for obviousness under § 103 must take into consideration the invention as a whole; that is, one must consider the particular problem solved by the combination of elements that define the invention. *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 1143, 227 USPQ 543, 551 (Fed. Cir. 1985). The Examiner must, as one of the inquiries pertinent to any obviousness inquiry under 35 U.S.C. § 103, recognize and consider not only the similarities but also the critical differences between the claimed invention and the prior art. *In re Bond*, 910 F.2d 831, 834, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990), *reh'g denied*, 1990 U.S. App. LEXIS 19971 (Fed. Cir. 1990). Further, the Final Office Action must provide specific, objective evidence of record for a finding of a suggestion or motivation to combine reference teachings and must explain the reasoning by which the evidence is deemed to support such a finding. *In re Sang Su Lee*, 277 F.3d 1338, 61 USPQ2d 1430 (Fed. Cir. 2002). Further yet, the fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990); MPEP § 2143.01. Finally, the Examiner must avoid hindsight. *In re Bond* at 834.

D) Discussion of the rejection of claims 10-11 under 35 U.S.C. § 103(a) as being obvious in view of the proposed combination of Chip et al. in view of Debabrata et al.

Claims 10-11 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Chip et al. ("The Coreware Methodology: building a 200 Mflop processor in 9 man month's") in view of Debabrata et al. ("A 600 MHz half-bit level pipelined accumulator-interleaved multiplier accumulator core"). Appellants respectfully traverse the rejection of claims 10-11 because the Final Office Action fails to state a *prima facie* case of obviousness with respect to claims 10-11.

The proposed combination of Chip et al. and Debabrata et al. fails to teach or suggest each of the elements included in claims 10-11.

Claims 10-11 depend from claim 8, and therefore include all the elements of claim 8. Claim 8 recites, "a multiplier coupled to receive interleaved operands and to produce a product; and a multi-threaded accumulator coupled to the multiplier to receive the product." As stated above in connection with claim 8, Chip et al. fails to teach or suggest a multiplier coupled to "receive interleaved operands," and fails to teach or suggest a "multi-threaded" accumulator coupled to the multiplier to receive the product, as recited in claim 8.

The additionally cited document Debabrata et al. fails to remedy the deficiency. Debabrata et al. on page 501 states, "The MAC architecture consists of a multiplier core to produce the products of the two numbers and an accumulator to add together these products." However, Appellants' representatives fail to find in Debabrata et al. a teaching or suggestion of a multiplier coupled to "receive interleaved operands," or a teaching or suggestion of "multi-threaded accumulator coupled to the multiplier to receive the product," as recited in claim 8. Thus, neither Chip et al. nor Debabrata et al., either alone or in combination, teach or suggest all of the elements of claims 10-11, and so the Final Office Action fails to state a *prima facie* case of obviousness with respect to claims 10-11.

In addition to failing to disclose al of the elements included in claims 10-11, the Final Office Action fails to state a proper basis for forming the proposed combination of Chip et al. and Debabrata et al.

The Final Office Action on pages 4-5 states, "Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to replace the mantissas in carry-save format as seen in Debabrata et al.'s disclosure into Chip et al.'s disclosure because it would enable to increase the system performance (e.g. page 502 last two lines and page 503 first two lines)."

Appellants respectfully disagree. The cited portion of Debabrata et al. states, "Addition of 2 logical bits of the operand requires a 4 → 2 adder. Hence, the clock period cannot be less than the delay of a 4 → 2 compressor. This will be referred to as a *Carry-Save Accumulation (CSA) bottleneck. The CSA bottleneck affects the throughput.*" (Emphasis added).

Therefore, the cited portion of Debabrata et al. describes Carry-Save Accumulation as a "bottleneck" that "affects the throughput." The Final Office Action on page 4 admits that Chip et al. fails to disclose "the mantissa is in carry-save format." Thus, Chip et al. is not concerned with Carry-Save Accumulation. Appellants respectfully submit that one or ordinary skill in the art would not be motivated to add a feature of Debabrata et al. that is disclosed as a "bottleneck" to the disclosure of Chip et al., which does not concern a mantissa in carry-save format.

Thus, the statements in the Final Office Action in support of making the proposed combination of Chip et al. with Debabrata et al. fail to show the desirability of making the proposed combination, and thus fail to meet the requirements as recited in the case law quoted above. By failing to meet these requirements, the Final Office Action fails to state a *prima facie* case of obviousness with respect to claims 10-11.

For at least the reasons stated above, Appellants respectfully request reversal of the rejection, and reconsideration and allowance of claims 10-11.

E) Discussion of the rejection of claims 12-14, 17-18, and 24-30 under 35 U.S.C. § 103(a) as being obvious in view of the proposed combination of Chip et al. in view of Choquette.

Claims 12-14, 17-18, and 24-30 were rejected under 35 U.S.C. § 103(a) as being obvious over Chip et al. in view of Choquette (U.S. Pat. No. 6,480,872). Appellants do not admit that Choquette is prior art and reserve the right, as provided for under 37 C.F.R. 1.131, to "swear behind" Choquette. Appellants respectfully traverse the rejection of claims 12-14, 17-18, and 24-30.

The proposed combination of Chip et al. and Choquette fails to teach or suggest each of the elements included in claims 12-14, 17-18, and 24-30.

Claims 12-14 depend from claim 8, claims 17-18 depend from claim 16, and claims 24-30 depend from claim 23. Therefore, these dependent claims include all of the elements of the independent claims from which they depend. For reasons analogous to those argued above, Chip et al. fails to teach or suggest each of the elements recited in claims 8, 16, and 23.

The additionally cited document Choquette fails to remedy the deficiency. Choquette at column 4, lines 52-46 recites, "In operation, the multiply array 410 multiplies operand 1 ("op1") to operand 2 ("op2") from working register A and B as shown in FIG. 4, and passes the result of the multiplication to the first adder 412, the shifter 414, and the result register 418." However, Appellants' representatives do not find in, and the Final Office Action fails to point out in Choquette a teaching or suggestion of "interleaved operands" or a "multi-threaded accumulator coupled to the multiplier to receive the product" as recited in claim 8, or a teaching or suggestion of "the accumulator having intermediate registers to simultaneously hold partial results from each of the different threads" as recited in claim 16, or a teaching or suggestion of "the accumulator including sequential elements to provide a multi-threaded capability" as recited in claim 23.

Thus, neither Chip et al. nor Choquette, either alone or in combination, teach or suggest all of the elements of claims 8, 16, and 23. Therefore, the Final Office Action fails to state a *prima facie* case of obviousness with respect to claims 12-14, 17-18, and 24-30.

In addition to failing to disclose all of the elements included in claims 12-14, 17-18, and 24-30 ,the Final Office Action fails to state a proper basis for forming the proposed combination of Chip et al. and Choquette.

On pages 5-6, the Final Office Action repeatedly states that the combination of Chip et al. with Choquette would have been obvious because the combination "would enable to properly producing the correct product-accumulation by shifting or aligning the product to the accumulation register." The Final Office Action relies on column 5, lines 5-9 of Choquette to support this statement. However, Choquette at column 5, lines 4-9 merely states,

> One of the two operands, commonly the smaller number of the two operands, is passed to the shifter 414 where the operand alignment is performed. Upon proper alignment between the operands, a FP addition is performed in the adder 416 and the result of the addition is stored in the result register 418.

Thus, there is no teaching or suggestion in the cited portion of Choquette to combine the shifter of Choquette with the matrix multiplication based on interleaved multiplier accumulator algorithm of Chip et al., as recited in the Abstract of Chip et al. Further, the inference of the statement made in the Final Office Action is that Chip et al. would be unable to produce the "correct" product-accumulation without the shifting of Choquette. However, Chip et al. on page 550, right hand column, beginning at line 1 states, "One of the keys to accomplishing the 200 MFlops peak performance is the interleaved Multiplier-Accumulator architecture." Therefore, the inference that Chip et al. requires shifting or aligning to produce a "correct" product accumulation appears to be counter to the disclosure in Chip et al.

In addition, on pages 7-8 the Final Office Action states that the combination would have been obvious because it would "enable to properly provide a desire format as

predetermined by the system," and because it would "increase the system performance by bypassing the alignment." Appellants note that the Final Office Action fails to point to any portions of either of the cited documents that supports these statements.

The Final Office Action on page 10 states,

> The examiner respectfully submits that the obvious reason to have an adder bypass path is to bypass the adder which would yield less time or clock to produce the summation. Therefore, it would have been obvious to an ordinary skill in the art at the time the invention is made to have a bypass path in order to increase the system performance.

However, the Final Office Action provides no references to support these statements. Without such support, the Final Office Action fails to meet the requirements of providing specific, objective evidence of record for a finding of a suggestion or motivation to combine reference teachings and must explain the reasoning by which the evidence is deemed to support such a finding - as found in the prior art and not based on Appellants' disclosure. By failing to meet these requirements, the Final Office Action fails to state a *prima facie* case of obviousness with respect to claims 12-14, 17-18, and 24-30.

For at least the reasons stated above, Appellants respectfully request reversal of the rejection, and reconsideration and allowance of claims 12-14, 17-18, and 24-30.

8. SUMMARY

For at least the reasons argued above, claims 8-9, 15-16, and 19-23 were not properly rejected under 35 U.S.C. § 102(b) as being anticipated by Chip et al., claims 10-11 were not properly rejected under 35 U.S.C. § 103(a) as being unpatentable over Chip et al. in view of Debabrata et al., and claims 12-14, 17-18, and 24-30 were not properly rejected under 35 U.S.C. § 103(a) as being unpatentable over Chip et al. in view Choquette.

It is respectfully submitted that the art cited does not render the claims anticipated or obvious, and that the claims are patentable over the cited art. Reversal of the rejection and allowance of the pending claims is respectfully requested.

Respectfully submitted,
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Name Amy Moriarty

Signature

CLAIMS APPENDIX

1-7. (Canceled)

8. (Rejected) An integrated circuit comprising:
a multiplier coupled to receive interleaved operands and to produce a product; and
a multi-threaded accumulator coupled to the multiplier to receive the product.

9. (Rejected) The integrated circuit of claim 8 further comprising a control circuit to interleave input interleaved operands from different operand streams into the multiplier.

10. (Rejected) The integrated circuit of claim 8 wherein the multi-threaded accumulator is configured to sum floating point numbers having mantissas in carry-save format.

11. (Rejected) The integrated circuit of claim 10 wherein the multi-threaded accumulator includes at least one intermediate register to facilitate accumulating two interleaved product streams simultaneously.

12. (Rejected) The integrated circuit of claim 8 further comprising a floating point conversion unit coupled between the multiplier and the multi-threaded accumulator to convert the product from a first floating point representation to a second floating point representation.

13. (Rejected) The integrated circuit of claim 12 wherein the first floating point representation includes an exponent field having a least significant bit weight of one, and the second floating point representation includes an exponent field having a least significant bit weight of thirty-two.

14. (Rejected) The integrated circuit of claim 13 wherein the multi-threaded accumulator circuit includes at least one constant shifter to conditionally shift a mantissa thirty-two bit positions.

15. (Rejected) The integrated circuit of claim 8 wherein the integrated circuit is a circuit selected from the group comprising a processor, a memory, a memory controller, an application specific integrated circuit, and a communications device.

16. (Rejected) An accumulator circuit to accept operands from different threads interleaved in time, the accumulator having intermediate registers to simultaneously hold partial results from each of the different threads.

17. (Rejected) The accumulator circuit of claim 16 further comprising:
a constant shifter prior to a first intermediate register; and
a multiplexor subsequent to the first intermediate register.

18. (Rejected) The accumulator circuit of claim 17 further comprising:
an adder circuit prior to a second intermediate register; and
a second multiplexor subsequent to the second intermediate register.

19. (Rejected) The accumulator circuit of claim 16 wherein the operands are floating point numbers in IEEE single precision format.

20. (Rejected) The accumulator circuit of claim 16 wherein the operands are floating point numbers in a floating point format other than IEEE single precision format.

21. (Rejected) The accumulator circuit of claim 16 wherein the floating point numbers include exponent fields with a least significant bit weight other than one.

22. (Rejected) The accumulator circuit of claim 21 wherein the floating point numbers include exponent fields with a least significant bit weight equal to thirty-two.

23. (Rejected) A multi-threaded floating point multiply-accumulator circuit comprising:

a multiplier to produce a product; and

an accumulator coupled to receive the product from the multiplier, the accumulator including sequential elements to provide a multi-threaded capability.

24. (Rejected) The multi-threaded floating point multiply-accumulator circuit of claim 23 further comprising a floating point conversion unit to convert the product from a first exponent weight to a converted product with a second exponent weight.

25. (Rejected) The multi-threaded floating point multiply-accumulator circuit of claim 24 wherein the accumulator is configured to produce a present sum from the converted product and a previous sum having the second exponent weight.

26. (Rejected) The multi-threaded floating point multiply-accumulator circuit of claim 25 further comprising a post-normalization unit to convert the present sum to a floating point resultant having the first exponent weight.

27. (Rejected) The multi-threaded floating point multiply-accumulator circuit of claim 23 wherein the accumulator includes:

an adder path; and

an adder bypass path.

28. (Rejected) The multi-threaded floating point multiply-accumulator circuit of claim 27 wherein the multiplier is configured to produce a product with an exponent weight of one.

29. (Rejected) The multi-threaded floating point multiply-accumulator circuit of claim 28 further comprising a floating point conversion unit to convert the product from an exponent weight of one to an exponent weight of thirty-two.

30. (Rejected) The multi-threaded floating point multiply-accumulator circuit of claim 29 wherein the accumulator is configured to accumulate numbers in carry-save format.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.